TECHNICAL BULLETIN # 103

Interconnecting PIKA Cards Using MVIP and H.100

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Software Version: MonteCarlo v5.6 and greater

Product(s): Daytona PCI, PrimeNet PCI, PrimeNet MM PCI

Purpose: This document contains a testing procedure to confirm correct cabling and settings when interconnecting PIKA cards with an MVIP and H.100 connectors.

Hardware Description

The Daytona PCI is a PCI card which supports enhanced compliant MVIP bus/512 timeslots and is CTBus (H.100) compatible. The CTBus has been physically connected with the MVIP bus. Please refer to Table 1 for the mapping of the two buses.

The PrimeNet PCI is a PCI card with MVIP and H.100 connectors. However, only the MVIP connector is fully functional. The H.100 connector does not have the full channel or CT Bus speed capabilities of the H.100 spec.

The PrimeNet MM PCI is a fully H.100 compliant PCI card. There is no MVIP connector on this board. Since the CT Bus has been designed to support easy inter-operation with telecom buses such as MVIP-90, it can communicate with an MVIP card using the H.100 Cable.

Definitions

H.100 Compatible: A card that can connect to the H.100 bus but does not have full 4096 channel switching capability. These cards typically use jumpers or software control to allow installers to configure the system.

H.100 Compliant: A card that can connect to the H.100 bus and has full 4096 channel switching capability. These cards may have internal resources that use some of the MVIP bus channels to perform their functions.

Stream Number	MVIP Bus Stream Number	CTBus Stream Number
0	Dso0	CT-D0
1	Dso1	CT-D2
2	Dso2	CT-D4
3	Dso3	CT-D6
4	Dso4	CT-D8
5	Dso5	CT-D10
6	Dso6	CT-D12
7	Dso7	CT-D14
8	Dsi0	CT-D1
9	Dsi1	CT-D3
10	Dsi2	CT-D5
11	Dsi3	CT-D7
12	Dsi4	CT-D9
13	Dsi5	CT-D11
14	Dsi6	CT-D13
15	Dsi7	CT-D15

Table 1: Mapping of the MVIP bus and CTbus on the Daytona card

Hardware Installation

Due to the inconsistent spacing between the Daytona PCI H.100 connector and the PrimeNet MM PCI H.100 connector, a relatively long CTbus cable is required. The PrimeNet PCI is connected with the Daytona PCI card through a MVIP cable. Figure 1 illustrates how the three boards are connected in one chassis.

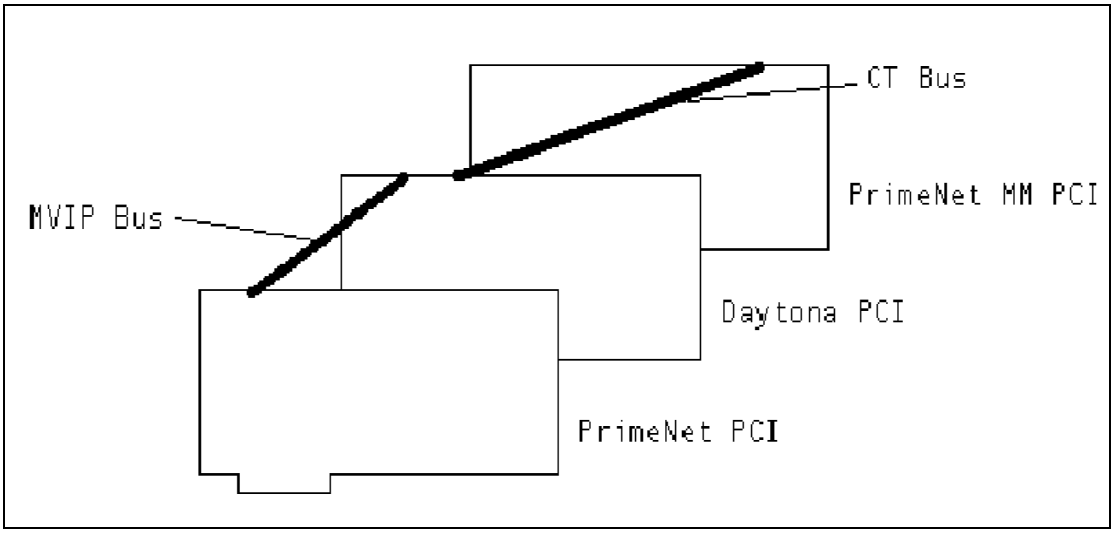

Figure 1. Recommended Cable Connections for Pika Cards

Software Configuration

1. Before starting your application, please make sure that the following devices (Control Panel -> Devices) have started. Please refer to Table 2 for the required devices for each card.

Board Name	Required Devices
Daytona PCI	PikaPCI
PrimeNet PCI	PikaPCIDSP PrimeNet
PrimeNet MM PCI	PikaPCIDSP563 PikaOctal

Table 2: Required device drivers for each card

2. Start MCSetup to detect the boards in the system and configure each installed board. Set either the PrimeNet PCI or the Daytona PCI as Master for the Bus Clock Mode. Set the other two cards to Slave mode for the Bus Clock Mode. Select the PrimeNet MM PCI card. Set the Bus Speed to '2Mbps' and the Clock Source to 'MVIP-4MHz'.

3. Run MCTest to verify if the bus connection has been set up. The following are the MCTest commands (in bold) and their results.

```
[MCTest window]
Ready.
v                  // describe boards in the system
B#  Type           Trunks          Phones   Dports         DSPs
--   ------------          ------   ------         ------  ----
 0  Daytona PCI     0   7          8  23          None     2
 1  PrimeNet PCI   24  69          None    None     2
 2  PrimeNetMM PCI 70 115          None    None             2
Ready.

Ready.
TD 0-115           //  TD <port>[-<port>]      VP stream & timeslot description
  0: Board 0 DSP 0 Stream 18 Timeslot  0 Mask 0x1f
  1: Board 0 DSP 0 Stream 18 Timeslot  2 Mask 0x1f
PK_VP_GetResourceDesc -102
…
 24: Board 1 DSP 0 Stream 19 Timeslot  1 Mask 0x1f
PK_VP_GetResourceDesc -102
…
 70: Board 2 DSP 0 Stream 32 Timeslot  0 Mask 0x1f
 71: Board 2 DSP 0 Stream 32 Timeslot 32 Mask 0x1f
 72: Board 2 DSP 0 Stream 32 Timeslot 64 Mask 0x1f
 73: Board 2 DSP 0 Stream 32 Timeslot 96 Mask 0x1f
PK_VP_GetResourceDesc -102
…
Ready.

Ready.
e 0  //  enable all detection on DSP port 0 (it's on DSP 0 of Board 0 --- Daytona PCI)
Ready.
e 24 //  enable all detection on DSP port 24 (it's on DSP 0 of Board 1 --- PrimeNet PCI)
Ready.
e 70 //  enable all detection on DSP port 70 (it's on DSP 0 of Board 2 --- PrimeNet MM)
Ready.
C+ d0  d24          // High level calls: d = dsp(default);
                    // C+ [dlc]<port> [dlc]<port> : connect two ports full duplex
                    // Connect dsp 0 <=> dsp 24
Ready.
```



```
t 0 9                       //   play a DTMF 9 with DSP port 0
Ready.
DSP @ 24 --- 9966532: DTMF_KEY_DOWN 9 8520       // the DTMF has been detected by port
                                                 // 24 which means the connection
                                                 // between port 0 and port 24 has been
                                                 // successfully set up
DSP @  0 --- 9961844: TGEN_TONE_PLAYED 0x9 0x0
DSP @ 24 --- 9966532: DTMF_ENERGY_LEVEL 48857843
DSP @ 24 --- 9966532: DTMF_KEY_UP 9 84

Ready.
t 24  9
Ready.
DSP @  0 --- 9961844: DTMF_KEY_DOWN 9 14868
DSP @  0 --- 9961844: DTMF_ENERGY_LEVEL 49051947
DSP @  0 --- 9961844: DTMF_KEY_UP 9 84
DSP @ 24 --- 9966532: TGEN_TONE_PLAYED 0x9 0x0

Ready.
C- d0  d24
Disconnect dsp 0 and dsp 24
Ready.

Ready.
C+ d0  d70
Connect dsp 0 <=> dsp 70
Ready.

T 0 9

Ready.
DSP @ 70 --- 9971428: DTMF_KEY_DOWN 9 32767
DSP @  0 --- 9961844: TGEN_TONE_PLAYED 0x9 0x0
DSP @ 70 --- 9971428: DTMF_ENERGY_LEVEL 48755038
DSP @ 70 --- 9971428: DTMF_KEY_UP 9 84

Ready.
t 70 9
Ready.
DSP @  0 --- 9961844: DTMF_KEY_DOWN 9 32767
DSP @  0 --- 9961844: DTMF_ENERGY_LEVEL 9860503
DSP @  0 --- 9961844: DTMF_KEY_UP 9 84
DSP @ 70 --- 9971428: TGEN_TONE_PLAYED 0x9 0x0

Ready.
C- d0  d70
Disconnect dsp 0 and dsp 70
Ready.

Ready.
C+ d24  d70
Connect dsp 24 <=> dsp 70
Ready.
t 24 9
Ready.
DSP @ 70 --- 9971428: DTMF_KEY_DOWN 9 27660
DSP @ 24 --- 9966532: TGEN_TONE_PLAYED 0x9 0x0
DSP @ 70 --- 9971428: DTMF_ENERGY_LEVEL 48826218
DSP @ 70 --- 9971428: DTMF_KEY_UP 9 84

Ready.
t 70 9
Ready.
DSP @ 24 --- 9966532: DTMF_KEY_DOWN 9 32767
DSP @ 24 --- 9966532: DTMF_ENERGY_LEVEL 9875020
DSP @ 24 --- 9966532: DTMF_KEY_UP 9 84
DSP @ 70 --- 9971428: TGEN_TONE_PLAYED 0x9 0x0

Ready.

// End of MCTest sample
```

